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Original Research Article

Experimental Validation of Zero-Crossing Detection Sinusoidal Pulse-Width Modulation for Grid-Synchronised Inverters in Renewable Energy Systems

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ABSTRACT

This article presents a synchronization control of a sinusoidal voltage from a single-phase inverter powered by a photovoltaic chain, with the sinusoidal voltage of the electrical network. The control is based on the principle of a phase-locked loop. This elaborate control does not necessarily use the blocks of a phase-locked loop, but it exploits its fundamental condition of constant phase difference and also the only resulting consequence that manifests itself in the frequency equality between the inverter voltage and the electrical network voltage. The voltage at the output of the inverter is synthesized from the sinusoidal voltage of the electrical network according to a succession of simultaneous operations performed on this sine wave. Indeed, the sine wave of the network is made accessible for measurement by control electronics. Then, a shaping (square signal) of the sine wave is carried out by zero comparison; the comparator changes state at each zero-crossing detection of the sine wave. On each rising edge of the square signal, a train of width-modulated pulses is started which controls the single-phase inverter by the sinusoidal pulse width modulation control which synthesizes the signal with the same frequency as the network. The algorithm of this command is implemented in an 8-bit microcontroller. An inverter from the photovoltaic chain developed in the laboratory was tested at the standard grid frequency (50 Hz) and at other frequencies (50 Hz to 80 Hz) to evaluate the system's ability to track frequency variations that may occur in practice due to grid disturbances. The manufactured inverter, equipped with the proposed phase-locked loop, successfully follows the electrical network. The steady-state frequency and phase errors remain below 1%, and the synchronization loop is established within 25 ms. The experimental results confirm the synchronization of the inverter to the power grid over a wide frequency range. Compared to classical synchronization techniques, often more complex to develop, the proposed phase-locked loop is a simple approach and suitable for implementation on standard microcontrollers controlling photovoltaic inverters under rapidly changing operating conditions.

KEYWORDS

Grid synchronisation, Renewable energy, Zero-crossing detector, Phase-locked loop, Inverter, Sinusoidal PWM.

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INTRODUCTION

The increasing use of renewable energy sources , in particular photovoltaic (PV) systems, is an essential solution to reduce greenhouse gas emissions and ensure sustainable electricity production [1]. However, the large-scale integration of these systems into power grids raises several planning, operational and management challenges [2]. Microgrids and distributed generation systems require reliable power electronic interfaces, such as DC-DC converters to regulate the power from PV panels [3], and the inverters to convert this energy into grid-compatible alternating current [4].

Inverters play a crucial role in the quality of injected energy [5]. They use pulse width modulation (PWM) techniques to control the output voltage and frequency by modulating signals applied to power switches [6]. There are two different strategies for modulation : unipolar modulation, which is characterised by low switching losses and reduced harmonic noise [7], and bipolar modulation, simpler but produced more losses and harmonics [8]. In order to further improve signal quality, advanced techniques are frequently employed such as spatial vector modulation (SVPWM) and sinusoidal modulation (SPWM) are widely used [9], [10].

The frequency, phase, and amplitude of the inverter output signal must be precisely synchronised with the network while maintaining the total harmonic distortion (THD) low in order to satisfy grid integration standards [11]. A proper sine wave at the inverter's output similar to that of the electrical grid's characteristics is ensured by the two signals being synchronised.

Phase-locked loop (PLL) is the most commonly used method for synchronizing inverters with the network [12]. This allows the inverter to produce an output voltage with a frequency equal to the network's frequency and a constant phase difference. The significant problem with PLLs is the locking area (frequency range) and achieving a fast loop response time. Apart from these two conditions (locking and fast detection), the PLL remains sensitive to perturbations and transient variations and can diverge. To overcome these limitations, many variations have been developed over the past 20 years.

Golestan *et al.* [13] introduced SOGI-FLL (Second-Order Generalized Integrator – Frequency Locked Loop), while Zhang *et al.* [14] enhanced SOGI-PLL to improve distortion rejection. Ranjan et al. [15] proposed the DSOGI-PLL, effective in unbalanced networks. Liu *et al.* [16] studied the SRF-PLL, widely adopted but sensitive to continuous shifts. Ortega and Milano [17] compared several variants (Lag-PLL, LPF-PLL [18], MAF-PLL [19]) and highlighted their respective compromises. The E-PLL [15] was designed to improve stability under too severe conditions. More recently, Prakash *et al.* [20] proposed an improved version of the SOGI-PLL with better disturbance rejection capability.

Despite their efficiency, these advanced approaches often require complex mathematical calculations and high-performance processors (DSP, FPGA), which limits their adoption in low-cost systems [14]–[20]. Therefore, the development of simple, robust and cost-effective synchronization techniques remains an open research need.

This work is part of the framework to propose a synchronization strategy for single-phase PV inverters, based on zero crossing detection (ZCD) [21] combined with SPWM [9].

Unlike classical PLL methods, this work adopts a path that involves only a zero-crossing detector (zero comparator) to obtain a square-wave signal of the same frequency as the grid. An 8-bit, general-purpose microcontroller then receives this sinusoid-shaped square-wave signal and generates the SPWM control used to drive a single-phase PV inverter.

This work is organized by designing a PV system that joins a 180 W peak power PV panel to a single-phase H-bridge inverter via a power adaptation structure. The purpose of this design is to:

Synthesize a sinusoidal waveform, at the output of the inverter charged by resistive load, with the same characteristics as those of the electrical network (same frequency and phase and same amplitude) by applying the ZCD synchronization technique with the SPWM.

Transfer the power, which exceeds the needs of the load, by redirecting it to the adaptation stage upstream from the inverter, towards an electrolyser that absorbs any excess power delivered by the PV generator and transforms it into hydrogen gas production through water electrolysis phenomenon.

The rest of this article is organized as follows: section 2 presents the system architecture and the design of the inverter used. Section 3 describes the proposed synchronisation strategy detailing the SPWM control and ZCD. Section 4 reports and discusses experimental validation. Finally, section 5 summarizes the conclusions and proposes future research perspectives.

PROPOSED SYSTEM

The proposed system aims to maintain grid compatibility while ensuring effective energy management between the PV generator, electrolyser, and inverter The following section describes the system structure in detail, with particular focus on the inverter design used for synchronisation with electrical grid.

System in Blocks

Figure 1 illustrates the full architecture of a PV chain that is intended to produce a sinusoidal waveform at its final output with properties similar to those of the single-phase electrical grid. The chain consists of:

- A PV panel producing 180 W under standard test conditions (1000 W/m² and 25 °C).
- An adaptation block composed of:
  - A Buck DC/DC converter, previously designed and dimensioned to operate at 100 kHz. This converter is equipped with a local MPPT control of the Perturb and Observe (P&O) type [22], [23], which maximizes the PV power and transfers it to the total system load. The total load consists of the inverter's final load and an auxiliary load represented by an electrolyzer that generates hydrogen gas. The electrolyzer has the ability to tolerate voltage and current fluctuations across its terminals without affecting its operation, thereby consuming the surplus energy exceeding the inverter's needs to produce hydrogen.
  - A Boost converter, connected between the electrolyzer and the inverter. This regulation stage specifically ensures a stable voltage at the inverter input [24], allowing it to generate an AC output with an effective value slightly higher than that of the grid voltage.
- An inverter stage that converts the DC power into AC power meeting the nominal voltage and current requirements of the load. The inverter is supplied by the DC bus regulated at 24 V and is controlled by a SPWM control, producing an alternating signal which, after LC filtering, becomes a clean sinusoidal waveform matching the grid in amplitude, frequency, and phase. This stage constitutes the main focus of this work.

The main advantage of this inverter structure lies in its nested dual-control mechanism: the PWM command is fully embedded within a square-wave signal derived from the grid's sinusoidal voltage. The PWM switching sequence begins only when the control unit receives the rising edge of this square-wave signal. This design enables a simple and flexible synchronization method, as the synthesis of the sinusoidal inverter output starts simultaneously with the detection and shaping of the grid waveform without requiring a feedback delay. Consequently, the inverter output follows the grid sinusoid in both frequency and phase without a conventional feedback loop that could slow down the system response.

The ZCD-based PLL developed in this work differs fundamentally from conventional PLLs in terms of internal structure but ultimately fulfils the same purpose: ensuring continuous tracking of the grid's frequency and phase for proper inverter synchronization.

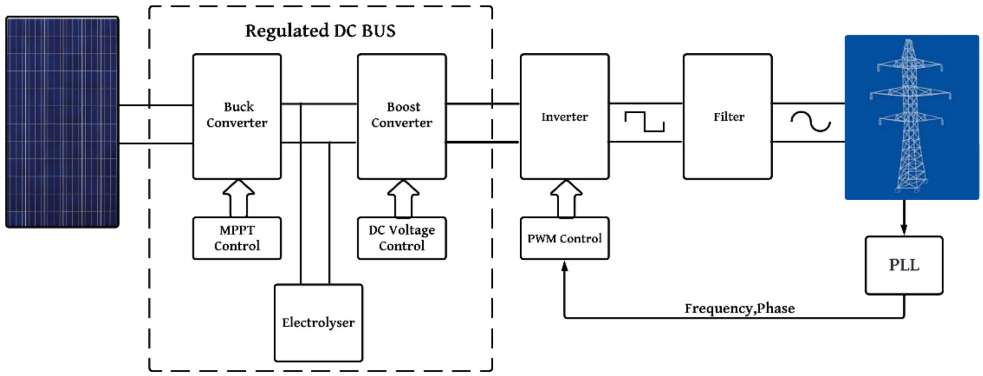

Figure 1. Block diagram of a PV system synchronised to the grid by the PLL

Inverter Design

PV systems convert solar energy into DC, typically at low voltage, while most electrical devices operate on AC at 230 V or 110 V. PV inverters therefore play a crucial role by transforming the DC power generated by PV panels into AC power, enabling its injection into the electrical grid or its use to supply various electrical appliances and machines.

Figure 2 shows the electrical schematic of the full-bridge inverter used in this design, consisting of four MOSFET switches labelled S1, S2, S3, and S4. The inverter input is supplied by the DC bus from the PV chain, while its output generates an alternating current intended either to feed an AC load or to be injected into the grid. The gates of the MOSFET transistors (switches) are driven by PWM signals modulated using a square-wave signal derived from the grid sinusoid (a pulse train embedded within a square waveform).

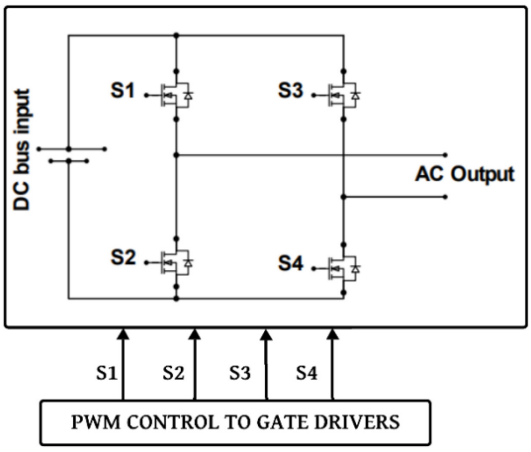

Figure 2. Full H-bridge inverter

The switching frequency was set to 500 Hz to minimize current ripples and obtain a regularly sinusoidal waveform.

A galvanic isolation was implemented between the control and power sections using optocouplers and gate drivers (A2211, IR2113) to protect the control circuitry from overvoltage and faults originating in the power stage. This configuration also enhances the operational safety and reliability of the overall system.

SYNTHESIS OF THE ZERO-CROSSING DETECTION PHASE-LOCKED LOOP

A control strategy based on a ZCD-PLL-SPWM has been developed in order to achieve reliable grid synchronisation. This section describes the principle of the proposed method and its implementation within the inverter control structure.

Principle of the Zero-Crossing Detection Method

The developed synchronization strategy is based on the synthesis of a simplified PLL, which differs from conventional architectures. Unlike traditional PLLs composed of a phase detector, a low-pass filter, an oscillator, and a feedback loop, the proposed version combines a ZCD circuit, a simple comparator of the grid sinusoidal voltage at 0 V, providing a square-wave signal at the same frequency as the grid, and a SPWM circuit derived from the grid waveform. The square-wave signal is then sent to an 8-bit Arduino microcontroller for further processing and control.

Sinusoidal Pulse Width Modulation Control for the Inverter

The SPWM is used for inverter control. This section presents the principle of the method as well as the steps for its digital implementation on an Arduino Uno microcontroller, indicating the main control parameters ensuring stable operation and correct synchronization with the grid.

Principle of the algorithm The code controls the switches of the full-bridge inverter by generating two PWM signals phase-shifted by 180. The flowchart in **Figure 3** summarises the main steps of the process.

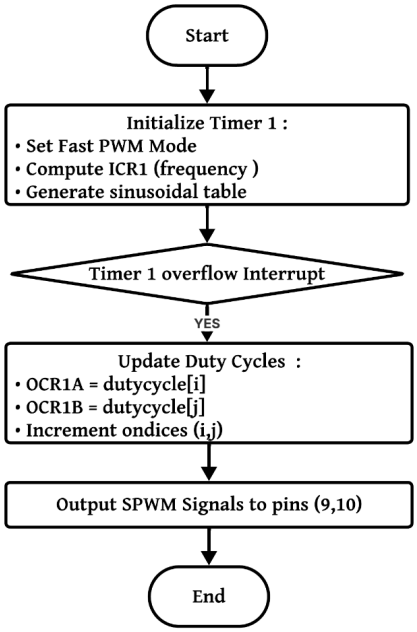

Figure 3. Implemented algorithm of the SPWM for the H-bridge inverter

By using this equation to determine the duty cycle values from the sine function, the reference wave is produced:

$$duty\ cycle\ i = \left(1 + \sin\frac{2\pi i}{n}\right)\frac{TOP}{2} + 0.5 \quad (1)$$

where are: *I* the table index (0 to *n*−1), *n* - number of samples per period, and *TOP* maximum value of the Timer counter.

The PWM frequency is determined by the configuration of the ICR1 register from the following equation:

$$TOP = \frac{F_{\mathrm{CPU}}}{f_{\mathrm{PWM}}} - 1 \quad (2)$$

where F_{CPU}=16 MHz: clock frequency of the microcontroller.

Therefore, the PWM frequency can be written as:

$$f_{PWM} = \frac{F_{CPU}}{TOP + 1} \tag{3}$$

The second PWM signal starts at halfway through the sine table. Thus, to achieve a 180° phase shift, the following equation is used:

$$j = \frac{n}{2} + i \tag{4}$$

The AC output voltage is determined by the difference between the two PWM signals for i and j variables:

$$V_{AC}(t) = V_{DC}(dutycyle_i(t) - dutycyle_j(t)) \tag{5}$$

Control Parameters and Implementation The digital implementation of the SPWM control was carried out on an Arduino Uno microcontroller, setting the main control parameters summarized in **Table 1**. These parameters include the fundamental frequency of the grid, the PWM switching frequency, the number of samples per period, the duty cycle calculation as well as the phase shift between the PWM signals.

Table 1. Control parameters used in the implementation

Parameter	Value	Description
Fundamental signal frequency (f_{signal})	50 Hz (nominal)	Reference grid frequency
PWM frequency (f_{PWM})	500 Hz	Switching frequency used for validation
Samples per period (n)	50	Discretisation of sinusoidal reference
Duty cycle i	Eq. (1)	Computed per sample, scaled to TOP = 31,999
Phase shift	180°	Between the two complementary PWM signals

This method, implemented using a microcontroller, offers the following advantages:

SPWM enables the generation of output voltages that closely resemble a sinusoidal waveform, with reduced harmonic distortion, thereby significantly improving signal quality. It is easy to implement on widely available microcontrollers and microprocessors, such as the ATmega328P used in the Arduino board.

SPWM is well suited for controlling the switches of a full-bridge (H-bridge) inverter, as the two complementary PWM signals ensure diagonal switch control and prevent simultaneous operation of switches on the same leg.

Microcontroller-Based Implementation of the Synchronisation Technique

The implementation of the ZCD-PLL within the microcontroller represents a key stage in achieving precise and stable synchronisation between the inverter and the electrical grid. This section details the digital realisation of the proposed control algorithm, its structure, and its integration into the microcontroller environment to ensure accurate frequency and phase tracking.

Principle of the algorithm The operation of the ZCD-PLL in the system, after the network signal has been converted into a square wave, is structured in three main stages, as illustrated in **Figure 4**.

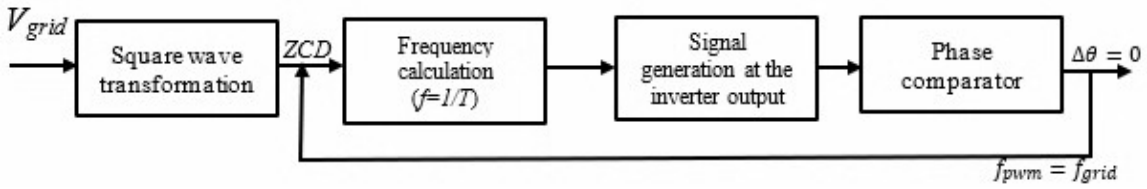

Figure 4. Block diagram of the proposed ZCD-PLL

Each rising edge triggers the PhaseLock interrupt routine, which records the current time and calculates the time interval T between two successive zero crossings. Based on this interval, the instantaneous frequency of the network is determined according to the relationship $f=1/T$. On the microcontroller side, these events are captured using an external interrupt configured in the code as follows:

attachInterrupt(digitalPinToInterrupt(2), PhaseLock, RISING);

The internal modulation frequency of the system is continuously compared to the measured frequency. If there is a deviation, the ICR1 register of Timer 1 is used to dynamically modify the PWM switching frequency. The SPWM algorithm creates two complementary PWM signals, each of which controls one of the inverter's two diagonal switches, by estimating the grid's frequency and phase. The DC bus voltage is subsequently transformed by the inverter into an AC waveform that is in phase and frequency synchronisation with the grid. The system continuously monitors the grid frequency and compensates for any deviations.

Finally, an LC filter removes high-frequency harmonics from the PWM signal, producing a clean sine wave suitable for grid coupling.

The overall control process is summarised in **Figure 5**, which illustrates the ZCD–PLL–SPWM algorithm implemented in the Arduino microcontroller.

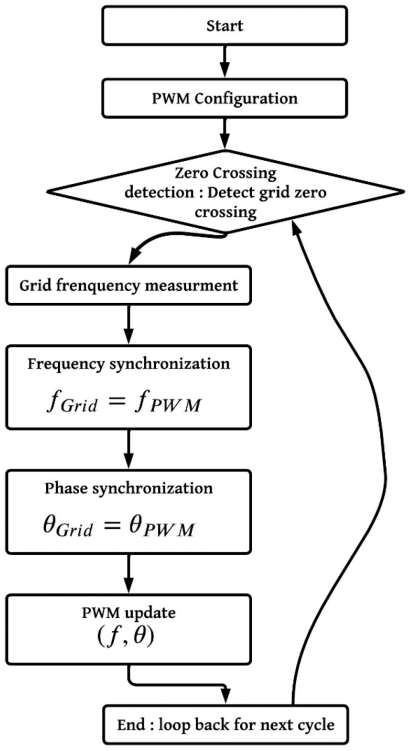

Figure 5. ZCD_PLL_SPWM algorithm implemented in the microcontroller

Synchronisation Accuracy Metrics In order to evaluate the performance of the proposed system, four key parameters were selected. These indicators are used to verify compliance with network code requirements and ensure that the inverter remains properly synchronized with the electrical grid. The parameters evaluated include phase error, frequency deviation, THD and reset time after a disturbance [25].

1. The phase error is obtained by measuring the time difference (Δt) between the zero-crossings of the grid signal and the inverter output. It is expressed as:

$$\Delta\phi = 360° \times \frac{\Delta t}{T} \tag{6}$$

Where T is the grid signal period.

2. The frequency deviation quantifies the difference between the inverter output frequency and the grid frequency:

$$\Delta f = f_{\text{inv}} - f_{\text{grid}},\ \varepsilon_f(\%) = 100 \times \frac{|\,\Delta f\,|}{f_{\text{grid}}} \tag{7}$$

where ε_f represents the relative error.

3. The harmonic content of the filtered inverter output voltage is evaluated using Fourier analysis. THD is calculated as:

$$THD = \frac{\sqrt{\sum_{k=2}^{\infty} V_k^2}}{V_1} \times 100\% \tag{8}$$

where V_1 is the RMS value of the fundamental component and V_k the RMS of the k^{th} harmonic.

4. The re-locking time is defined as the duration required for the PLL to re-establish synchronisation after a disturbance or a sudden variation in grid frequency. It is expressed as:

$$T_{\text{lock}} = t_1 - t_0 \tag{9}$$

where t_0 is the instant of disturbance and t_1 the instant at which stable synchronisation is regained.
These parameters enable the system's compliance with network code requirements in terms of stability, voltage quality and resynchronisation speed to be assessed.

EXPERIMENTAL PROCEDURE

A test bench is designed to validate the power distribution in the PV system and the proposed synchronisation approach, by executing the diagrams in Figure 6.

The installation comprises a PV panel delivering 180 W of power under standard conditions (1000 W/m², 25 °C), an Arduino microcontroller for real-time control, as well as a single-phase 220/24 V transformer and galvanic isolation and adaptation circuits to lower the mains voltage to 5 V to ensure the safety of the electronic components.

A four-channel Tektronix TBS2000B oscilloscope (used in relaxed time base mode) and an acquisition system based on LV25-P (voltage) and LA55-P (current) sensors were used for

real-time monitoring and analysis of electrical signals, as well as for measuring the power generated by the PV and consumed in the system.

Adaptation Structure

The adaptation unit consists of a 100 kHz DC/DC converter equipped with a P&O MPPT algorithm that optimises the power extracted from the PV generator and transfers it to the loads: electrolyser and alternating load (inverter output).

A cylindrical electrode electrolyser, placed downstream of the Buck, accepts tolerance to variations in current and voltage at its terminals. This electrolyser does not act as a load shedding device that dissipates energy in the form of Joule heating. The electrolyser is introduced at this exact point to maintain the optimal operating point and convert the absorbed energy into hydrogen production, which is considered an energy vector from PVs.

Finally, a boost converter controls the voltage at 24 V which is then converted to 220 V to match the grid amplitude, ensuring a stable power supply to the inverter and a functional separation between hydrogen production and AC conversion.

Inverter Control

Inverter control is based on synchronisation using the ZCD method.

This architecture ensures phase locking, frequency tracking and waveform stability between the inverter output voltage and the grid reference signal.

Several test scenarios were developed to evaluate the ZCD synchronisation method on the PV system and inverter, particularly in response to frequency variations.

In practice, these variations were introduced using a low-frequency generator (LFG) replacing the electrical grid and providing a variable reference signal. By gradually varying the frequency of the LFG from 50 Hz to 60 Hz, then to 80 Hz, it was possible to analyse the ability of the ZCD-SPWM control algorithm to continuously track and adapt to these changes.

The tests were carried out using two types of sinusoidal reference sources:

Synchronisation of the inverter with the grid at a fixed mains frequency of 50 Hz;

Continuation of the inverter's synchronisation with the low-frequency generator (50 Hz, 60 Hz and 80 Hz) simulating the variable-frequency mains.

The evaluation focused exclusively on the ability of the ZCD control algorithm to maintain the synchronisation of the inverter with the grid, in particular phase alignment, frequency tracking and waveform tracking to ensure that it can be injected into the grid.

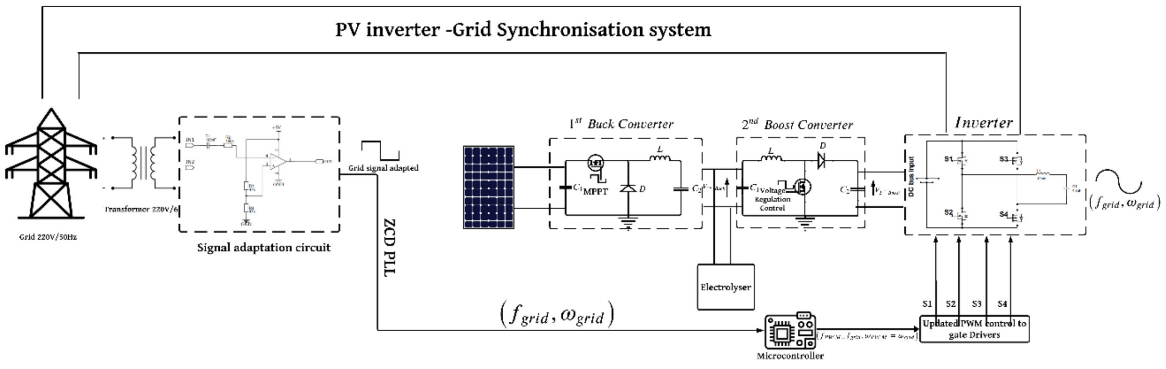

Figure 6. Block diagram of the grid synchronisation system with the inverter

RESULTS AND DISCUSSION

The tests are carried out in the laboratory for different frequency values, focusing on the phenomenon of synchronisation, from the inverter output to the sine wave on the electrical grid.

Analysis of Power Balance and Energy Distribution in the System

As shown in **Figure 7**, the power delivered by the PV generator varies between 20 W and 90 W depending on fluctuations in irradiance. The tests were carried out with a 100 Ω load, under unstable sunlight conditions in order to assess the stability of the system. The electrolyser absorbs most of the available power (approximately 10 W to 70 W), in line with the system's main function of hydrogen production, while the finale load consumes relatively low power 5 W depending on the load used and remains stable, in order to show that the synchronisation phenomenon has always occurred.

Despite rapid variations in irradiance (between 200 and 600 W/m²), the energy distribution remains balanced and overall losses do not exceed 10%, mainly due to losses in the converters and the inverter. Furthermore, **Figure 8** shows that the DC bus voltage, regulated by the boost converter, remains stable at around 24 V, ensuring a constant power supply to the inverter and continuous synchronisation even in the presence of environmental fluctuations.

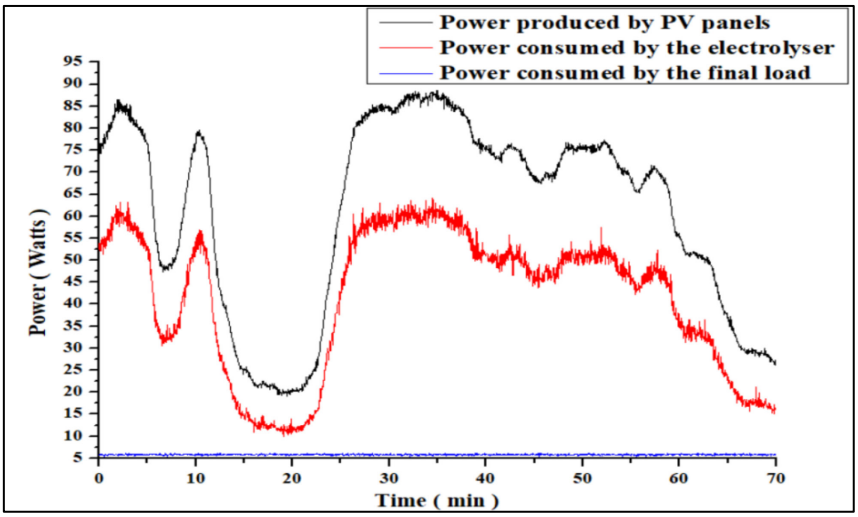

Figure 7. System Performance: PV Power Generation and Consumption

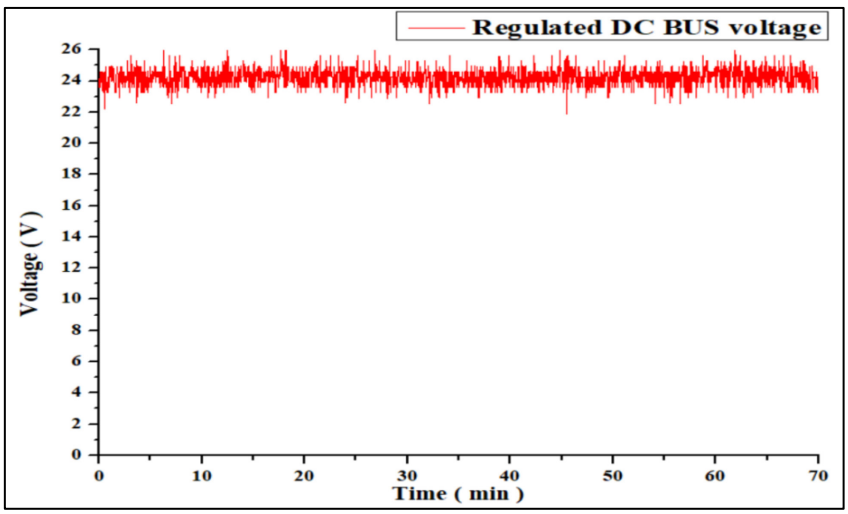

Figure 8. Controlled Voltage at the output of the boost converter

Analysis of Photovoltaic-Inverter System Performance and Synchronisation

The SPWM-modulated AC signal (**Figure 9**), once filtered by the LC filter (**Figure 10**), produces a clean sine wave that complies with grid wave quality standards. This is because the filtering process removes all harmonics above 50 Hz.

In order to evaluate the stability of the proposed synchronisation method, step frequency variations were applied using an LFG, with values of 50 Hz, 60 Hz and 80 Hz. The results, shown in **Figure 11** to **Figure 13**, demonstrate that the inverter maintains stable synchronisation during these frequency transitions. The inverter output voltage (blue trace) follows the reference signal (red trace), confirming the ability of the ZCD–PLL–SPWM control to track frequency variations.

Next, tests were carried out with the actual power grid. **Figure 14** illustrates the inverter output voltage before synchronisation, while **Figure 15** shows the PWM waveform after synchronisation has been established. **Figure 16** highlights the phase tracking process, during which the inverter voltage gradually locks onto that of the grid.

Finally, the filtered output voltage of the inverter is illustrated in **Figure 17**, which shows a high-quality sine wave that is precisely synchronised with the grid in terms of frequency, phase, and amplitude even when there are an unstable weather affecting irradiance

The grid reference signal is sinusoidal, according to oscilloscope measurements, while the inverter output before filtering exhibits a PWM waveform. The algorithm automatically adjusts the phase and switching frequency during synchronisation until the two signals are completely superposed. Following filtering, the output voltage aligns with the grid and takes the form of a stable sinusoidal waveform.

The ZCD control, implemented on an Arduino microcontroller, uses zero-crossing detection to directly extract phase and frequency information, reducing the complexity of processing and hardware. This approach is suitable for low-cost PV systems and applications requiring synchronisation for possible injection of PV current into the electricity grid.

Tests carried out for different reference frequencies (50 Hz, 60 Hz and 80 Hz) confirm the stability of the synchronisation and the system's ability to adapt to dynamic variations and changes in irradiance, while maintaining smooth and consistent operation.

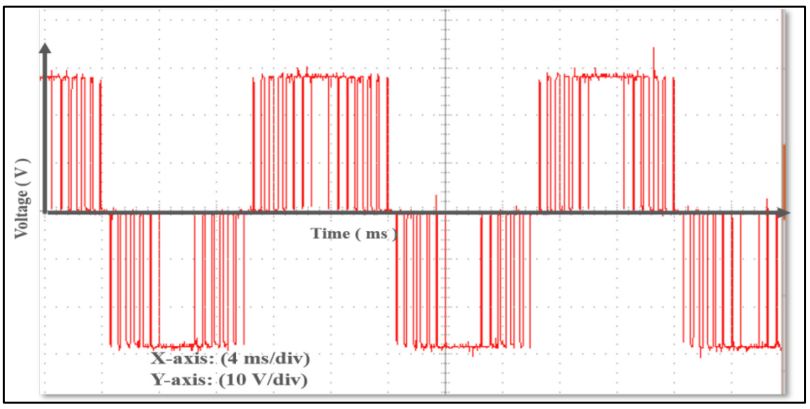

Figure 9. Inverter output voltage by unfiltered SPWM control

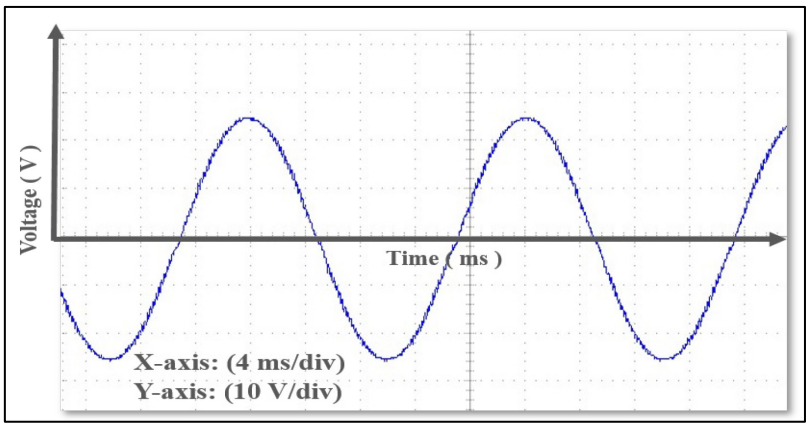

Figure 10. Inverter output with filtering

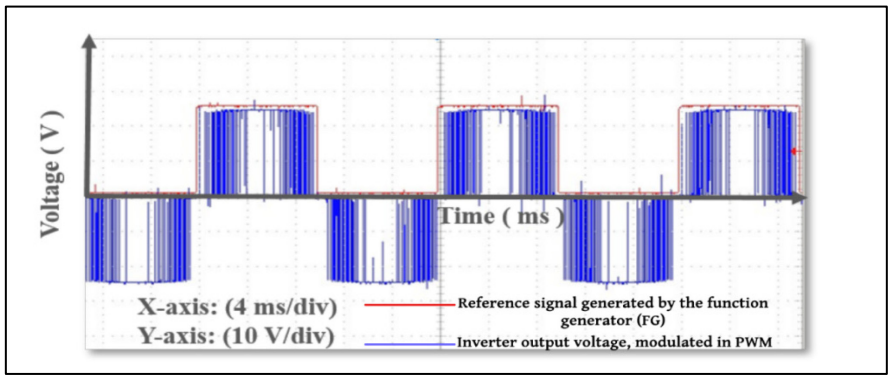

Figure 11. Inverter signal output synchronised with reference signal with frequency 50 Hz

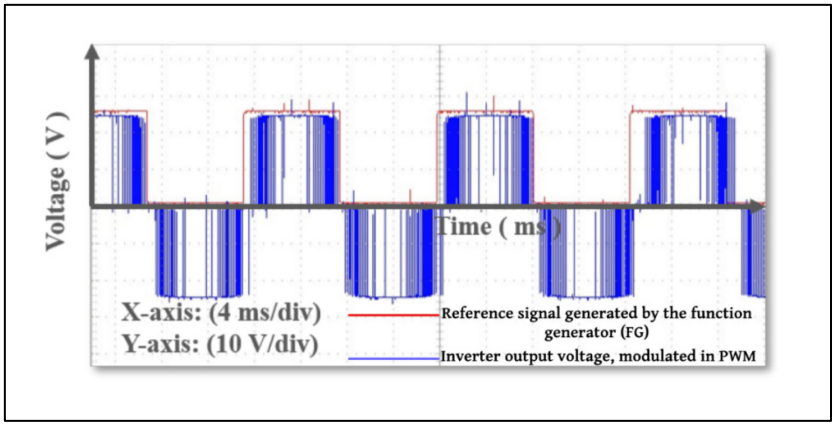

Figure 12. Inverter signal output synchronised with reference signal with frequency 60 Hz

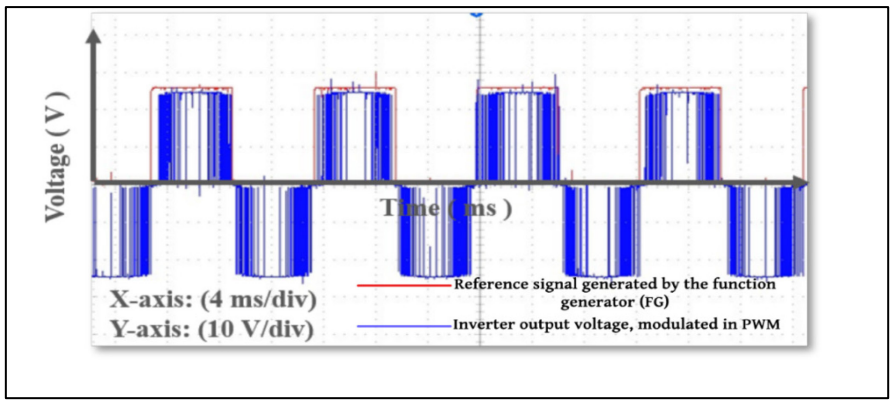

Figure 13. Inverter signal output synchronised with reference signal with frequency 80 Hz

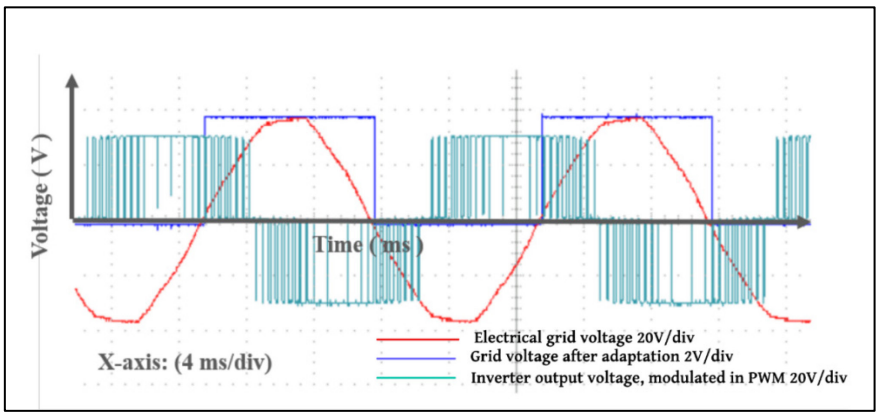

Figure 14. System not synchronised with the electrical grid

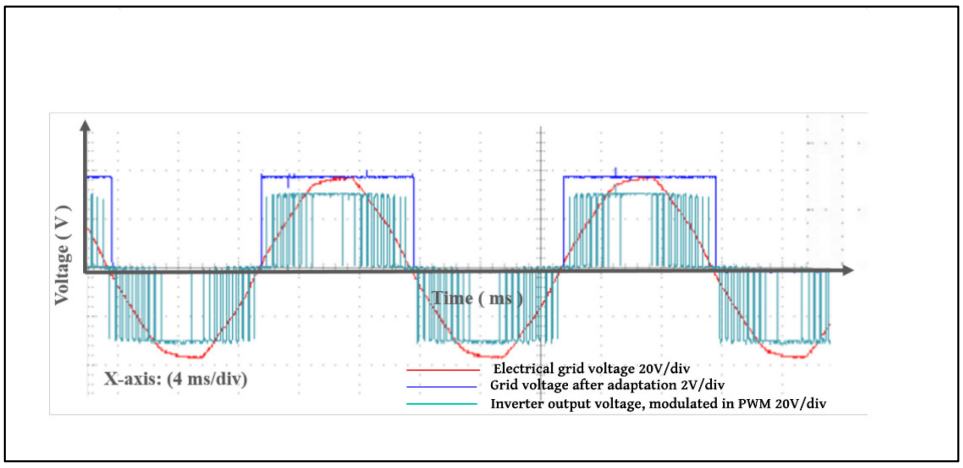

Figure 15. Inverter output and grid signal synchronised in phase and frequency

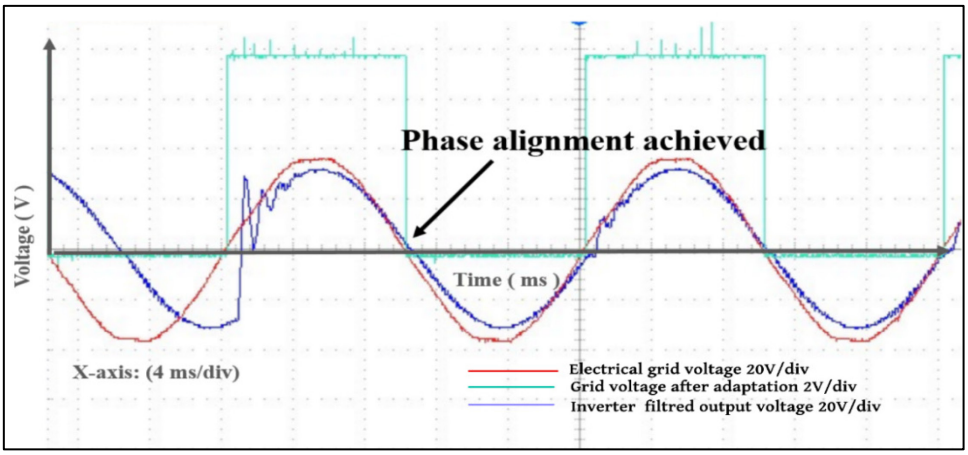

Figure 16. Phase alignment obtained through the proposed ZCD–PLL–SPWM synchronisation method

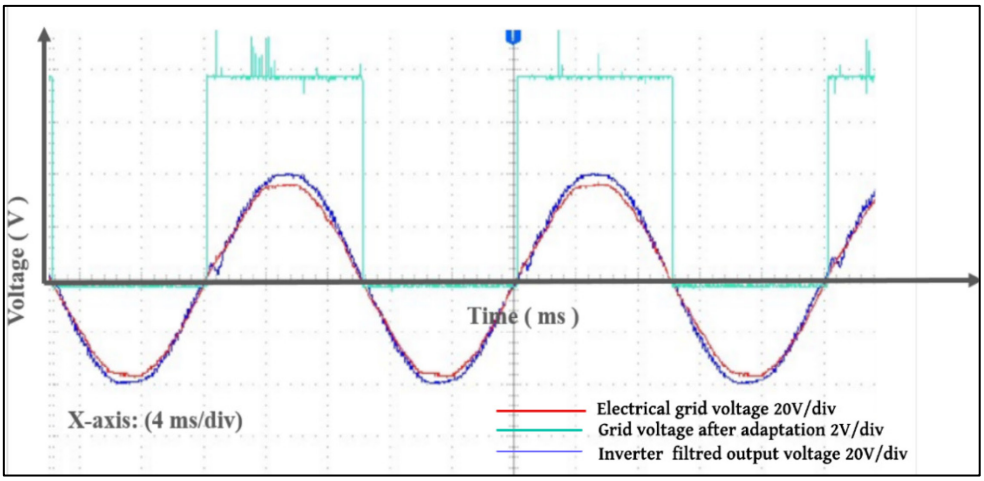

Figure 17. Filtered inverter output synchronised with grid signal in phase and frequency

Results Summary

The performance of the proposed ZCD synchronisation technique was evaluated using the accuracy indicators defined in the synchronisation accuracy metrics section.

The phase error, calculated according to eq. (6) from the measured time difference between the zero crossings of the grid and inverter signals, is approximately 0.9°, which is below the 1° limit commonly considered for stable grid integration.

The frequency deviation, determined according to eq. (7), is 0.05 Hz for a nominal grid frequency of 50 Hz and an inverter output frequency of 49.95 Hz, i.e. a relative error of 0.1%, below the tolerance of ±1%.

Spectral analysis of the output signal using fast Fourier transform indicates a THD of 0.68% after LC filtering by applying eq. (8), which is below the 5% threshold recommended by the IEEE 519 standard for grid-connected systems.

The re-locking time, obtained from eq. (9) after a frequency variation from 50 Hz to 60 Hz, is approximately 25 ms.

The main results are presented in **Table 2**, illustrating the compliance of the proposed system with the synchronisation requirements in terms of phase alignment, frequency tracking, harmonic distortion and stability.

Table 2. Summary of synchronisation performance metrics

Metric	Equation used	Result	Standard requirement
Phase error ($\Delta\varphi$)	Eq. (6)	0.9°	< 1°
Frequency deviation (Δf)	Eq. (7)	0.05 Hz (0.1%)	< ±1%
THD	Eq. (8)	0.68%	< 5%
Re-locking time	Eq. (9)	25 ms	< 50 ms

CONCLUSION

This article presents a new, simple synchronisation strategy for single-phase PV inverters, which differs significantly from conventional PLLs. Synchronisation between the electrical grid and the inverter is achieved by combining ZCD with SPWM. The proposed method allows phase and frequency locking without the use of any feedback loops requiring heavy calculations that delay the response time of the PV system to follow the electrical grid.

Experimental tests have shown that the system maintains a phase error of less than 1°, a frequency deviation of less than 0.1%, and a THD of 0.68%, with a re-locking time of approximately 25 ms during frequency variations. The system remained stable even when the reference frequency varied in steps from 50 Hz to 80 Hz.

Furthermore, tests carried out under varying irradiance conditions confirmed the PV system's ability to distribute energy between the electrolyser and the inverter. The boost converter maintained a stable DC bus voltage of around 24 V, even under fluctuating weather conditions. The results obtained show that the PV system is functioning as expected at all levels of design, in particular the smooth tracking of the inverter's sinusoidal voltage to that of the reference signals (grid or low-frequency generator simulating the grid):

Beyond the experiments conducted in this work, the ZCD technique can be extended to other high-power PV systems for possible connection to the electricity grid. The ZCD method can also be extended to all microgrid systems and decentralised installations and to any system producing direct current energy, in order to transform it into alternating current energy to synthesise a wave similar to that of the grid.

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NOMENCLATURE

F	generic frequency	[Hz]
F_{CPU}	micro-controller clock frequency	[Hz]
f_{Grid}	grid frequency	[Hz]
Δf	frequency deviation	[Hz]
F_{PWM}	PWM carrier frequenc	[Hz]
I	index of the sine-lookup table ($0 \rightarrow n-1$)	[-]
$ICR1$	input-capture register that sets f_{PWM}	[-]
J	index shifted by 180° ($i + n/2$)	[-]
N	number of samples per electrical period	[-]
TOP	maximum count value of the timer	[-]
T	period	[s]
T	time variable	[s]
THD	total harmonic distortion	[%]
T_{lock}	re-locking time after disturbance	[s]
Δt	time difference between two zero-crossings	[s]
V_g	RMS grid voltage	[V]
V_{AC}	RMS AC-line voltage (grid side)	[V]
V_{DC}	DC-link/bus voltage	[V]
V_{inv}	inverter output voltage	[V]

Greek letters

$\Delta\varphi$	phase error between inverter and grid	[°]
φ	instantaneous grid phase angle	[rad]
ω	angular frequency	[rad · s^{-1}]
ε_f	relative frequency error	[%]

Abbreviations

LFG	Low-Frequency Function Generator
LC	Inductor-Capacitor Filter
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
PLL	Phase Locked Loop
PV	Photovoltaic
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
ZCD	Zero Crossing Detection

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